REMARKS

The Office Action dated October 29, 2003 has been received and carefully noted. The above amendments to the claim and specification, and the following remarks, are submitted as a full and complete response thereto.

By this Amendment, Applicants have amended claims 1, 8, 13, 24, 28, 32, 52 and 57 to more particularly point out and distinctly claim the present invention. No new matter has been added. In view of the following remarks, reconsideration and allowance of these claims is respectfully requested.

CLAIM OBJECTIONS

Claim 24 was objected to because of minor informalities. This claim has been amended to correct these minor informalities. Thus, Applicants respectfully request the withdrawal of this objection.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

Claims 1-4, 6, 8, 9, 11, 13-15, 18-21, 23-25, 28-30, 32-34, 37-40, 42-44, 47, 48, 52, 53 and 57-60 were rejected under 35 U.S.C. §102(e) as being anticipated by Muller et al. (U.S. Patent No. 6,021,132). The Office Action alleges that Muller teaches all of the limitations of the claimed invention. Applicants respectfully submit that the prior art cited in the Office Action fails to teach, suggest or disclose the features of the claimed invention.

Claim 1, upon which claims 2-12 are dependent, recites a memory structure, comprising an Address Resolution Table, a Packet Storage Table and a single buffer per

packet mechanism. The Address Resolution Table resolves addresses in a packet-based network switch. The Packet Storage Table is adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table. The single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted.

Claim 13, upon which claims 14-31 are dependent, recites a memory structure having a memory block. The memory block comprises an Address Resolution Table, a Transmit Resolution Table, a Transmit Descriptor Table and a single buffer per packet mechanism. The Address Resolution Table, having an associative memory structure, resolves addresses in a packet-based network switch. The Transmit Descriptor Table is associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table is adapted to receive a Table Descriptor Address and a Table Descriptor Value. The Packet Storage Table is adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion.

Claim 32, upon which claims 31-51 are dependent, recites a packet-based switch having a memory structure. The memory structure comprises an Address Resolution Table, a Transmit Descriptor Table, a Packet Storage Table and a single buffer per packet mechanism. The Address Resolution Table, having an associative memory structure, resolves addresses in a packet-based network switch. The Transmit Descriptor Table is

associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table is adapted to receive a Table Descriptor Address and a Table Descriptor Value. The Packet Storage Table is adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion. The single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted.

Claim 52, upon which claims 53-56 are dependent, recites a packet-based switch comprising an Address Resolution Table having a one-way associative memory structure and a Packet Data Buffer Table sharing a memory block with an Address Resolution Table. The packet-based switch also comprises a single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted.

Claim 57, upon which claims 58-60 are dependent, recites a packet-based switch, comprising an Address Resolution Table having a direct-mapped/one-way associative memory structure. The Address Resolution Table resolves addresses in a packet-based network switch. The packet-based switch also comprises a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted.

As a result of the claimed invention, a memory structure for resolving addresses in a packet-based network switch is provided. The present invention provides a single buffer per packet approach. Thus, one advantage of the present invention is significant bandwidth savings that can attributed to the one buffer per packet approach. The single buffer-per-packet technique enhances the feasibility of the bit-per-buffer free buffer pool tracking technique, as well, and the need to search a large buffer pool structure can be mitigated or eliminated. These advantages are not all inclusive but merely exemplars of some of the benefits of the invention.

Applicants submit that Muller fails to disclose or suggest the elements of the invention as set forth in the claimed invention, and thereby fails to provide the critical and nonobvious advantages that are provided by the invention. In order to anticipate a claim, it is well established that a reference must disclose every element of the claim. *Verdegaal Bros. V. Union Oil Co.,* 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.,* 9 USPQ2d (Fed. Cir. 1989).

Muller discloses a shared memory management in a switched network element. A shared memory manager for a packet forwarding device includes a pointer memory having stored therein information regarding buffer usage (e.g., usage counts) for each of a number of buffers in a shared memory. An encoder is coupled to the pointer memory for generating an output which indicates a set of buffers that contains a free buffer. The

shared memory manager further includes a pointer generator that is coupled to the encoder for locating a free buffer in the set of buffers. The pointer generator produces a pointer to the free buffer based upon the output of the encoder and the free buffer's location within the set of buffers.

Applicants respectfully submit that Muller fails to disclose or suggest each and every element of the claimed invention, as required for a rejection under 35 USC § 102. For instance, Muller fails to disclose or suggest a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted as recited in independent claims 1, 8, 13, 28, 32, 52 and 57. Support for this limitation can be found, for example, on page 6, line 30 through page 7, line 29 of the application..

Regarding claims 1 and 52, Muller also ails to disclose or suggest, at least, a Packet Storage Table adapted to receive a packet for storage in the packet-based network switch and sharing a preselected portion of memory with the Address Resolution Table and a Packet Data Buffer Table sharing a memory block with the Address Resolution Table. This feature is shown, for example, in Figure 1 and discussed on page 4, line 33 – page 5, line7 which explains that the Packet Data Storage Table 4 may be co-located with the Address Resolution Table 5. The Packet Data Storage Table 4 may share memory 3 with the ARL Table 5. However, the Office Action contends that the forwarding memory 113 corresponds to the ARL of the present invention and the shared memory manager

220 corresponds to the Packet Data Storage Table of the present invention. First, Applicants submit that Muller does not disclose or suggest an arrangement where the forwarding memory 113 and the shared memory manger 220 share a "memory block." Second, Applicants further submit that the forwarding memory 113 does not correspond to or suggest the ARL of the claimed invention and that the shared memory manager 220 does not correspond to or suggest the Packet Data Storage Table of the claimed invention.

Furthermore, regarding independent claims 13 and 32, Muller fails to disclose or suggest, at least, "a Packet Storage Table, the Packet Storage Table adapted to receive at least one of each of a Packet Data Address and a Packet Data Value." As discussed, for example, on page 6, lines 20-29, the present invention discloses a "preselected portion" of a packet destination as an index into the Address Resolution Logic (ARL) Table so that an address match can be resolved quickly and the packet passed to the appropriate port for transmission. However, Muller merely discloses a shared memory management that includes a pointer generator that is coupled to an encoder for locating a free buffer in a set of buffers. The Office Action alleges that the shared memory manager 220 in Muller corresponds to the Packet Storage Table in the claimed invention. Applicants respectfully disagree with this analysis because in the present invention, as discussed for example of page 10, lines 19-27, the data packets can be stored in the Packet Data Storage Table with a packet data address portion and a packet data value portion. As discussed above, the present invention uses a "preselected portion" of the packet. In

contrast, Muller states, in col. 6, lines 52-60, that the shared memory manager 220 provides a level of indirection by locally storing pointers to buffers that contain packet data rather than locally storing the packet data itself. In other words, the shared memory manager 220 merely stores pointers, but does not store a portion of the packet.

For at least these reasons, Muller fails to anticipate independent claims 1, 13, 32 and 52.

Claims 2-12 depend from claim 1, claims 14-31 depends from claim 13, claims 33-51 depend from claim 32 and claims 53-60 depend from claim 52 and are therefore allowable for the reasons that claims 1, 13, 32 and 52 are allowable, respectively, and for the specific limitations recited therein.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

Claims 5, 7, 10, 12, 16, 17, 22, 26, 27, 31, 35, 36, 41, 45, 46, 49-51 and 54-56 were separately rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. (U.S. Patent No. 6,021,132). The Office Action alleged that Muller discloses all of the elements of the claimed invention, with the exception of the specific limitations recited within each dependent claims. Applicants respectfully submit that Muller fails to teach, suggest or disclose the features of the claimed invention. Therefore, the rejection is respectfully traversed and reconsideration is respectfully requested for the reasons which follow.

Applicants submit that Muller fails to disclose the claimed invention for the reasons discussed above in reference to the Claim Rejections under 35 U.S.C. §102. In

particular, Muller fails to disclose a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per said individual packet and for enabling an execution of a single access in order to locate an entire packet to be transmitted as recited in independent claims 1, 8, 13, 28, 32, 52 and 57.

Since claims 5, 7, 10 and 12 depend from claim 1, claims 16, 17, 22, 26, 27 and 31 depend from claim 32, claims 35, 36, 41, 45, 46 and 49-51 depend from 32 and claims 54-56 depend from claim 52, these claims are allowable for the reasons that claims 1, 13, 32 and 52 are allowable, respectively, and for the specific limitations recited therein. Furthermore, Applicants respectfully submit that Muller neither discloses, as admitted by the Office Action, or suggests the specific limitations recited in these dependent claims. Rather, as discussed above, Muller relates to a shared memory management in a switched network element wherein the shared memory management includes a pointer generator for locating a free buffer in a set of buffers. Thus, Muller does not render the claimed invention obvious.

CONCLUSION

Claims 1-60 are pending. Applicants have amended the title of the invention. Applicants have amended claims 1, 8, 13, 24, 28, 32, 52 and 57 to more particularly point out and distinctly claim the present invention. No new matter has been added. Applicants submit that Muller fails to disclose or suggest the limitations of the claimed invention as discussed above. Thus, Applicants submit that certain clear and important

distinctions exist between the cited prior art and the claimed invention. Applicants submit that these distinctions are more than sufficient to render the claims of the invention unanticipated by and unobvious in view of the prior art. It is therefore requested that claims 1-60 be found allowable, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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Enclosures: